A 12 GHz 140K LOW NOISE GaAs FET AMPLIFIER

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A low noise GaAs FET amplifier provided with the noise temperature of less than 140K (NF: 1.71 dB) at -50°C over 11.7 ~ 12.2 GHz band was developed using GaAs FET's with a recess structure and MIC technology.

Introduction

Recent performance improvement of low noise GaAs FET's is remarkable and low noise GaAs FET amplifiers are extensively used for the microwave communications systems up to K-band. Although low noise GaAs FET amplifiers are widely used in the satellite communications systems, especially in 4 GHz band, parametric amplifiers are still used in 12 GHz band even for Domsat applications because of its their excellent noise temperature.

However, the parametric amplifiers are highly expensive and require complicated maintenance. There has been great demands to replace them by the low noise GaAs FET amplifiers which gives a lower cost, and compact and maintenance-free systems.

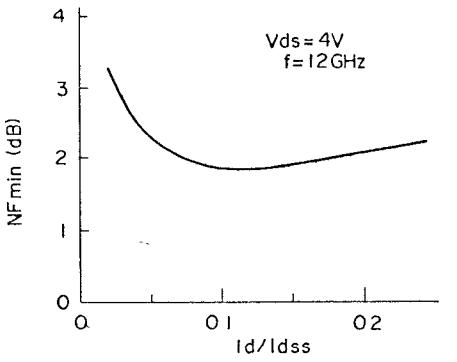
Development of super low noise GaAs FET's makes the noise performance of GaAs FET amplifiers closer to that of parametric amplifiers. This paper describes a 12 GHz low noise GaAs FET amplifier using newly developed recess structure low noise GaAs FET's which provides with less than 2.0 dB noise figure at 12 GHz. The noise temperature of the developed 12 GHz 2-stage amplifier is less than 140K when cooled down to -50°C. Overall noise temperature of 12GHz GaAs FET LNA (6-stage) shows to be enough to replace some of the parametric amplifiers.

Design and Circuit Configuration

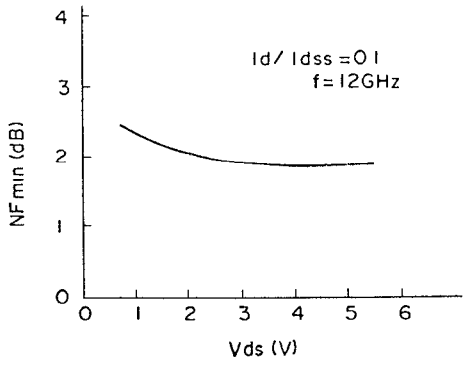
For the 12 GHz low noise GaAs FET amplifier, a super low noise GaAs FET NE137 was newly developed.

In order to improve the noise figure of the GaAs FET, a deep recess structure was adopted, because the source resistance of the GaAs FET with a deep recess structure was reduced to a half of that of a conventional flat type GaAs FET. The GaAs FET NE137 has 0.5 μm gate length. The noise figure was less than 2.0 dB at 12.0 GHz. This performance is better than the best value of the conventional flat type GaAs FET's with the same gate length.[1]

In the circuit design for the low noise amplifiers, the bias point to obtain a minimum noise figure must be determined. The relationships between the minimum noise figure NFmin and the normalized drain current Id/Idss is shown in Fig. 1a, where Id is the drain current and Idss the drain saturation current. The minimum noise figure is obtained at the vicinity of Id/Idss = 0.1. This characteristic of NFmin agrees with that computed by Pucel.[2] Fig. 1b shows the drain-source voltage Vds dependence of NFmin. For small value of Vds, NFmin decreases with the increase of Vds, and NFmin change little in Vds $\geq$ 4 V. From the above experimental results, the drain current is set at 10% of Idss and the drain-source voltage at 4 V.



(a) Drain current dependence of NFmin



(b) Drain-source voltage dependence of NFmin.

Fig. 1. Relationships between the minimum noise figure and d.c. bias

To broaden the bandwidth and to obtain minimum noise temperature, GaAs FET's used in unpackaged chip form are housed together with the internal matching circuits in a metal package by utilizing MIC technology.

The unit amplifier that is a 2-stage amplifier utilizing NE137 chips, was designed with the aid of computer optimization. Then the initial circuit was modified experimentally to obtain minimum noise figure.

The circuit construction of the unit amplifier is shown in Fig. 2. Two low noise GaAs FET NE137 chips are used for TR1 and TR2. MIC 1, MIC 2 and MIC 3 are the input, interstage and output internal matching circuit, respectively. Each internal matching circuit is composed of distributed constant elements formed on $A\ell_2O_3$ substrate and some lumped elements. The relative dielectric constant of $A\ell_2O_3$ substrate is 10.8 and the thickness is 0.635 mm. On each internal matching circuit pattern, several bonding lands are provided for adjustment by taking account of the variation of FET and circuit parameters.

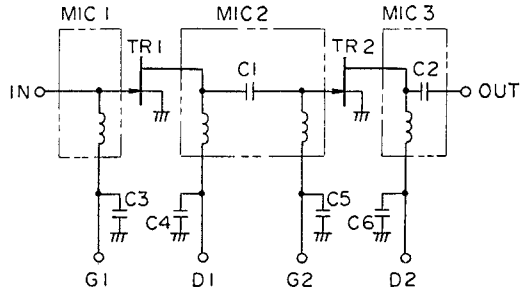


Fig. 2. Circuit construction of the unit amplifier

C1 and C2 are chip capacitors for dc-block, are soldered on the $A\ell_2O_3$ substrates. In the input internal matching circuit, no dc-block chip capacitor is used in order to reduce the circuit loss, because a chip capacitor has about 0.2 dB loss at 12 GHz.

The FET chips, the $A\ell_2O_3$ substrates and the bypass chip capacitors are mounted in a hermetically sealed metal package.

Fig. 3 show the block diagram of the 12 GHz low noise GaAs FET amplifier. The amplifier is constructed with a unit amplifier, two coaxial isolators and two waveguide-to-coaxial adapters. In this amplifier, no coaxial connector is used, because a pin contact of coaxial connector has 0.05 - 0.08 dB circuit loss, and the loss, particularly the loss of input circuit, must be reduced as much as possible. Therefore, the coaxial isolator and the waveguide-coaxial adapter is directly connected, and the coaxial isolator and the unit amplifier is connected with a 50-ohm micro-strip line formed on the teflon-fiberglass substrate.

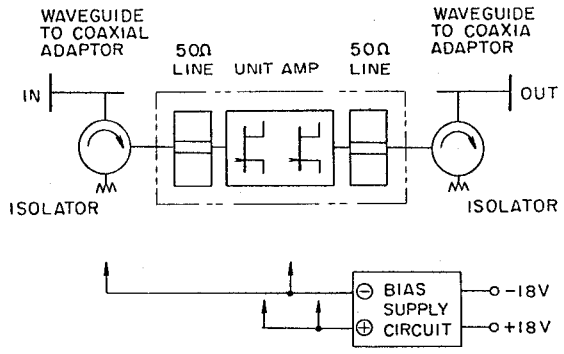


Fig. 3. Block diagram of the 12 GHz low noise GaAs FET amplifier

As the sources of FET's are grounded, two kinds of voltage power source +18 V and -18 V are employed for drain and gate bias, respectively. By the bias supply circuit, the drain and gate bias are adjusted to the minimum noise figure points.

An open circuit termination is used for the input isolator. The gate bias of the first stage FET is supplied through the open circuit termination. The dc-block in the input circuit is accomplished by the waveguide-to-coaxial adapter of input port.

Fig. 4 shows the external view of the 12 GHz low noise GaAs FET amplifier without the bias supply circuit.

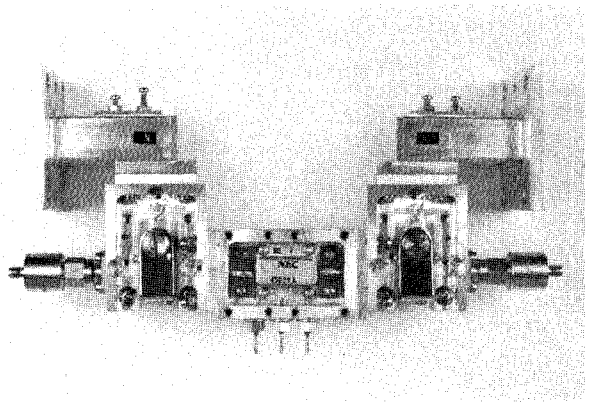


Fig. 4. External view of the 12 GHz low noise GaAs FET amplifier

Performance

Typical performance of the 12 GHz 2-stage low noise GaAs FET unit amplifier are shown in Fig. 5. The noise temperature at 25°C is less than 200K (NF: 2.28 dB) in the 11.7 ~ 12.2 GHz band and the gain is more than 17 dB. When the amplifier is cooled down to -50°C, the noise temperature is improved to less than 140K (NF: 1.71 dB) and the gain rises by 1 or 1.5 dB. Fig. 6 shows the calculated noise temperature reduction and measured data.[3]

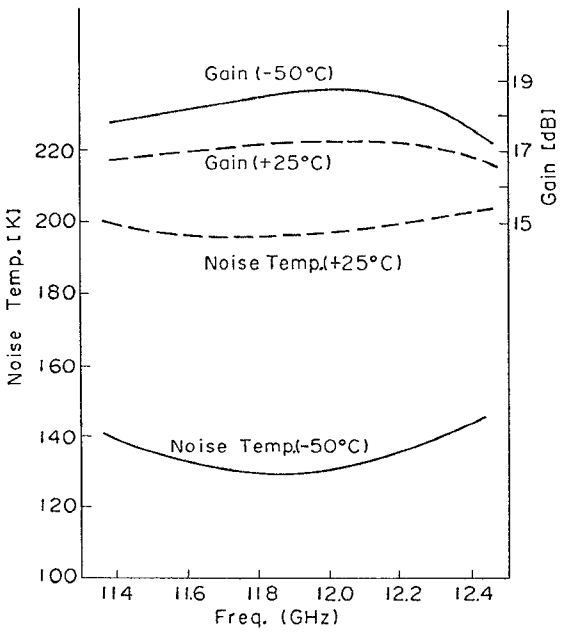


Fig 5. Gain and noise temperature of the 12 GHz low noise GaAs FET amplifier

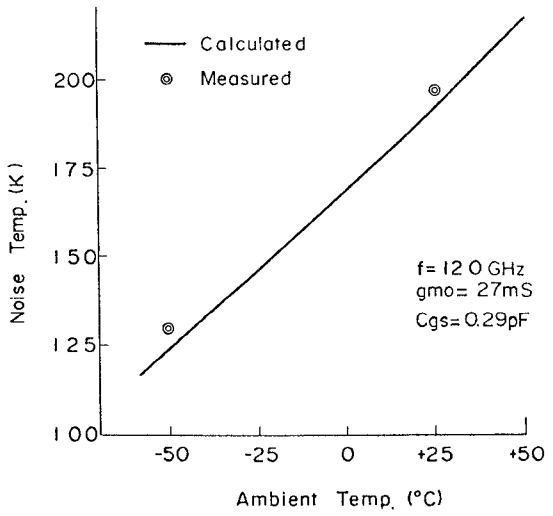


Fig. 6. Noise temperature versus ambient temperature

12 GHz GaAs FET LNA which consists of 3 unit amplifiers was constructed. The first unit amplifier was cooled to -50°C by the thermo-electric cooling technique and the succeeding two unit amplifiers were kept at 25°C. Overall noise temperature was less than 155K and the gain was approximately 51 dB.

This performance points out that the low noise GaAs FET amplifiers are able to take the place of the parametric amplifiers at 12 GHz band.

Conclusion

A 12 GHz low noise GaAs FET amplifier has been developed using GaAs FET's with a recess structure and MIC technology.

The noise temperature of the amplifier was less than 200K (NF: 2.29 dB) at 25°C, and 140K (NF: 1.71 dB) was achieved by cooling down at -50°C. This performance is enough for replacement of some of parametric amplifiers.

Acknowledgement

The authors wish to express their hearty thanks to Mr. R. Tamura, Mr. S. Yokoyama and Mr. M. Kajikawa of Microwave & Satellite Communications Division, and Dr. K. Ayaki and Dr. F. Hasegawa of Central Research Laboratories, for invaluable suggestions and encouragement throughout the development work of this amplifier. They are also grateful to Dr. T. Irie and many other engineers of Semiconductor Division for useful advices and cooperation.

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